WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

an FET, to be a protected element and comprising in turn a gate electrode, a source electrode, and a drain electrode, connected to operating region surfaces provided on a substrate, and a gate terminal, a source terminal and a drain terminal respectively connected to the electrodes; and

a protecting element, connected in parallel to any two of the terminals of the protected element and having an insulated region disposed between the two terminals of a first high concentration impurity region and a second high concentration impurity region;

the semiconductor device, wherein electrostatic energy applied between the two terminals of the protected element is discharged between the first and second high concentration impurity regions to thereby attenuate the electrostatic energy that reaches the two electrodes corresponding to the two terminals of the protected element to a level that does not exceed the electrostatic breakdown voltage between the two electrodes.

2. The semiconductor device of claim 1, wherein the electrostatic breakdown voltage of the protected element is improved by no less than 20V in comparison to prior to the connection of the protecting element.

3. The semiconductor device of claim 1, wherein the protecting element is disposed close to a bonding pad connected to at least one of the terminals of the protected element.

4. The semiconductor device of claim 1, wherein the protecting element is connected in the middle of the path from a bonding pad connected to a terminal of a protected element to an operating region.

5. The semiconductor device of claim 1, wherein one protecting element is disposed along at least one side of a bonding pad connected to the terminal of the protected element.

6. The semiconductor device of claim 1, wherein a plurality of the protecting elements are

provided and each is disposed along at least one side of one bonding pad connected to the terminal of the protected element.

7. The semiconductor device of claim 1, wherein the first high concentration impurity region is connected to a bonding pad connected to one terminal of the protected element or to a wiring that is connected to the bonding pad.

8. The semiconductor device of claim 1, wherein the first high concentration impurity region is a part of a connection means connecting a bonding pad, connected to one terminal of the protected element, to one electrode of the operating region.

9. The semiconductor device of claim 1, wherein the second high concentration impurity region is connected to a bonding pad connected to other terminal of the protected element or to a wiring that is connected to the bonding pad.

10. The semiconductor device of claim 1, wherein the second high concentration impurity region is a part of a third high concentration impurity region, disposed at the periphery of a bonding pad, connected to other terminal of the protected element, or a wiring connected to the bonding pad.

11. The semiconductor device of claim 1, wherein the protecting elements are disposed in plurality respectively close to bonding pads connected to other terminals of the protected element and the first high concentration impurity region of each of the plurality of protecting elements is a part of a connection means connecting a terminal and an operating region of the protected element.

12. A semiconductor device comprising:

as a protected element, a switching circuit, wherein first and second FET's, each provided with a source electrode, a gate electrode, and a drain electrode connected to operating region surfaces on a substrate, are formed, a terminal connected to a source electrode or a drain electrode in common of both FET's is used as a common input terminal, terminals connected to the drain electrodes or the source electrodes of the respective FET's are respectively used as first and second

output terminals, terminals connected to the gate electrodes of the respective FET's are respectively used as first and second control terminals, and control signals are applied to both of the control terminals to make, via resistors, which are connection means that connects both of the control terminals with the gate electrodes, one of the FET's turn on to form a signal path with the common input terminal and one of either first or second output terminal; and

a protecting element, connected in parallel between at least one of the control terminals and the input terminal of the protected element and having an insulated region disposed between a first high concentration impurity region and a second high concentration impurity region; and

wherein electrostatic energy, applied from the exterior between at least one control terminal and the common input terminal, is discharged between the first and second high concentration impurity regions to attenuate the electrostatic energy that reaches between electrodes respectively corresponding to at least one control terminal and the common input terminal to a level that does not exceed the electrostatic breakdown voltage between the electrodes.

13. The semiconductor device of claim 12, wherein the electrostatic breakdown voltage between said common input terminal and said one control terminal is improved by no less than 20V in comparison to prior to the connection of the protecting element.

14. The semiconductor device of claim 12, wherein the protecting element is connected in parallel between at least one of the control terminals and at least one of the output terminals of the protected element and the electrostatic breakdown voltage between the protected element is improved by no less than 20V in comparison to prior to the connection of the protecting element.

15. The semiconductor device of claim 12, wherein the protecting element is disposed close to at least the common input terminal.

16. The semiconductor device of claim 12, wherein the protecting element is connected within a path from a bonding pad, connected to at least one control terminal, to the gate electrode.

17. The semiconductor device of claim 12, wherein the protecting element is disposed along at least one side of a bonding pad to which the common input terminal is connected.

18. The semiconductor device of claim 12, wherein the protecting element is disposed along at least one side of a bonding pad to which the at least one output terminal is connected.

19. The semiconductor device of claim 12, wherein a plurality of the protecting elements are provided, each being disposed along at least one side of a bonding pad to which the common input terminal is connected.

20. The semiconductor device of claim 12, wherein the first high concentration impurity region is connected to a bonding pad, connected to at least one control terminal, or to a wiring connected to the bonding pad.

21. The semiconductor device of claim 12, wherein the first high concentration impurity region is a part of a resistor connecting a bonding pad, connected to at least one control terminal, and the gate electrode.

22. The semiconductor device of claim 12, wherein the second high concentration impurity region is connected to a bonding pad, connected to he common input terminal, or to a wiring connected to the bonding pad.

23. The semiconductor device of claim 12, wherein the second high concentration impurity region is part of a third high concentration, disposed at the periphery of a bonding pad of the common input terminal or a wiring connected to the bonding pad.

24. The semiconductor device of claim 12, wherein the protecting elements are disposed in plurality respectively close to a bonding pad, connected to the common input terminal, and bonding pads, each connected to at least one output terminal, and the first high concentration impurity region of each of the plurality of protecting elements is a part of a resistor connecting at least one control terminal and the gate electrode.

25. The semiconductor device of claim 1 or 12, wherein the electrostatic breakdown

voltage of the protected element is made no less than 200V.

26. The semiconductor device of claim 1 or 12, wherein the first and second high concentration impurity regions of the protecting element are separated by a distance through which electrostatic energy can be passed.

27. The semiconductor device of claim 1 or 12, wherein the first and second high concentration impurity regions are impurity regions of the same conduction type.

28. The semiconductor device of claim 1 or 12, wherein the first and second high concentration impurity regions are impurity regions of different conduction types.

29. The semiconductor device of claim 1 or 12, wherein the first and second high concentration impurity regions both have an impurity concentration that is approximately equivalent to that of the source region and that of the drain region that contact the source electrode and drain electrode.

30. The semiconductor device of claim 1 or 12, wherein the insulating region is an impurity implanted region provided in the substrate.

31. The semiconductor device of claim 1 or 12, wherein the insulating region is a part of a semi-insulating substrate.

32. The semiconductor device of claim 1 or 12, wherein at least one of either of the first and second high concentration impurity regions is connected with a metal electrode and the metal electrode is connected to a bonding pad, connected to a terminal of the protected element, or a wiring connected to the bonding pad.

33. The semiconductor device of claim 32, wherein the metal electrode forms a Schottky junction with a surface of the substrate that is positioned 0 μm to 5 μm to the outer side of an end part of the first and/or second high concentration impurity regions.

34. The semiconductor device of Claim 1 or 12, wherein the FET is a MESFET, a junction type FET, or an HEMT.